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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,300	12/15/2003	Yoshiharu Nakajima	SON-1697/DIV	4716

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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
02/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/734,300	NAKAJIMA ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 06 February 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-3,10-25,40-45 and 54-58*.
   Claim(s) withdrawn from consideration: *4-9,26-39,46-53 and 59-61*.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: please see attachment.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

Prabodh M. Dharia
Primary Examiner

1. **Status:** Please all replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 02-06-2008 under amendments and request for reconsideration, which have been placed of record in the file. Claims 1-3, 10-25, 40-45 and 54-58 are pending in this action. Claims 4-9, 26-39, 46-53 and 59-61 are cancelled.

Response to Amended Claims after final

2. Applicant's request for reconsideration and amendments with new claims received on 02-06-2008 are not entered, they do raise new issue and require further consideration and search, since they were not presented before final office action.

Response to Arguments

3. Applicant's arguments filed 02-06-2008 on the basis of request for reconsideration have been fully considered and they are not persuasive; however, they do require further consideration and search for new and amended claims as they were not presented before mailing of final office action.

4. Applicant has failed to respond to obvious type double patenting rejection where Claims 1-3,10-25, 40-45, and 54-58 are rejected on the ground of nonstatutory double patenting over claims 1-50 of U. S. Patent No. 6,664,943 B1 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

5. Applicant argues, Koyoma fails to teach or suggest, at least, "a digital-analog converter ... comprising 2n step select units connected across 2" reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the

n- bit digital data signal; wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area."

Examiner disagrees as Koyoma discloses a digital-analog converter circuit for converting (Col. 4, lines 60,61) an n-bit (n is an integer of 2 or more) digital data signal (Col. 4, Lines 62,63) comprising 2n step select units connected across 2n reference voltage lines (Col. 25, Line 5 to Col. 26, Line 3, Col. 5, Lines 15-63, n=2 bits and reference voltages are 2n=4 please see figure 2), each step select unit including n serially connected analog switches polarized to match the logic state of each data signal n bit (n is an integer of 2 or more), (Col. 5, Lines 15-63, Col. 4, Line 60 to Col. 5, Line 7 and there are two sets of n bits (2 sets of switches n-channel and p-channel are connected in series and polarized to match the logic state of each data signal; each sets of bits has four (or 2n) reference voltages; each set has one end connected to reference voltage and column line input) and 2n tone select units (Col. 4, Lines 61,62; each sets of bits has four (or 2n) reference voltages) respectively connected across the outputs of each of the 2n reference voltage lines bit of the n-bit digital data signal (Col. 25, Line 5 to Col. 26, Line 3, Col. 5, Lines 15-63, each set has one end connected to reference voltage and column line input; Col. 4, Lines 60-64, Col. 27, Lines 23-38, Col. 38, Line 56 to Col. 39, Line 39, teaches an example of 2n bits being 4 sets of reference voltages); wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area (please see figures 1, and 2 Col. 9, Line 62 to Col. 11, Line 28 discloses the four sets of transistors P-channel and N-channel connected in the series driven by tow bits of data signal inverted and non-inverted producing

four bits to provide 16 logical state. Further Koyama; Jun et al. discloses the Column line providing D/A conversion for display is connected to each of the four transistors in middle; n is an integer of 2 or more, Col. 5, Lines 15-63, Col. 4, Line 60 to Col. 5, Line 7 and there are two sets of n bits (2 sets of switches n-channel and p-channel are connected in series and polarized to match the logic state of each data signal; each sets of bits has four (or 2n) reference voltages; each set has one end connected to reference voltage and column line input providing and therefore the column lines are connected to each pair at the one end to an effective pixel area; as well as reference voltages are also connected at other end of the each pair of switching transistors).

The prior art of Butler teaches a level shift circuit having a CMOS latch cell as the basic structure (please see figures 15, 16, Col. 15, Line 59 to Col. 16, Line 5, Col. 16, Lines 42-62) and for converting a low voltage amplitude signal to a high voltage amplitude signal (Col. 16, Lines 20-62) comprising: a CMOS latch cell having two input sections, wherein a first resistor element is inserted respectively between each of the two signal sources and the two input sections of said CMOS latch cell and two signal sources (Col. 15, Line 59 to Col. 16, Line 62).

Combination teaches applicant's claimed invention and therefor they do obviate.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

7. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

/PRABODH DHARIA/

AU2629

Primary Examiner

February 14,2008